ABSTRACT OF THE DISCLOSURE

A circuit and method for correcting erroneous data in memory for pipelined reads. A memory controller includes a control unit, a storage unit and an error detection and correction unit. The control unit is configured to read data including an associated error correction code from a memory subsystem in response to a memory read request. The error detection and correction unit is coupled to receive the data and configured to determine whether an error exists in that data based upon the associated error correction code. The control unit is configured to store an indication in the storage unit that the data corresponding to the memory read request is erroneous. The control unit is further configured to detect the indication in the storage unit and to responsively perform a subsequent read of the data from the memory subsystem and to write a corrected version of the data back to the memory subsystem.